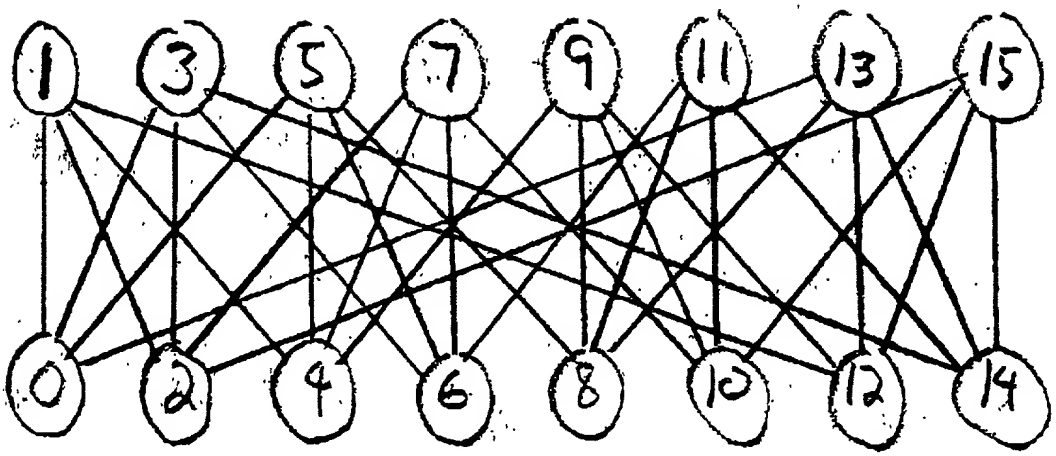
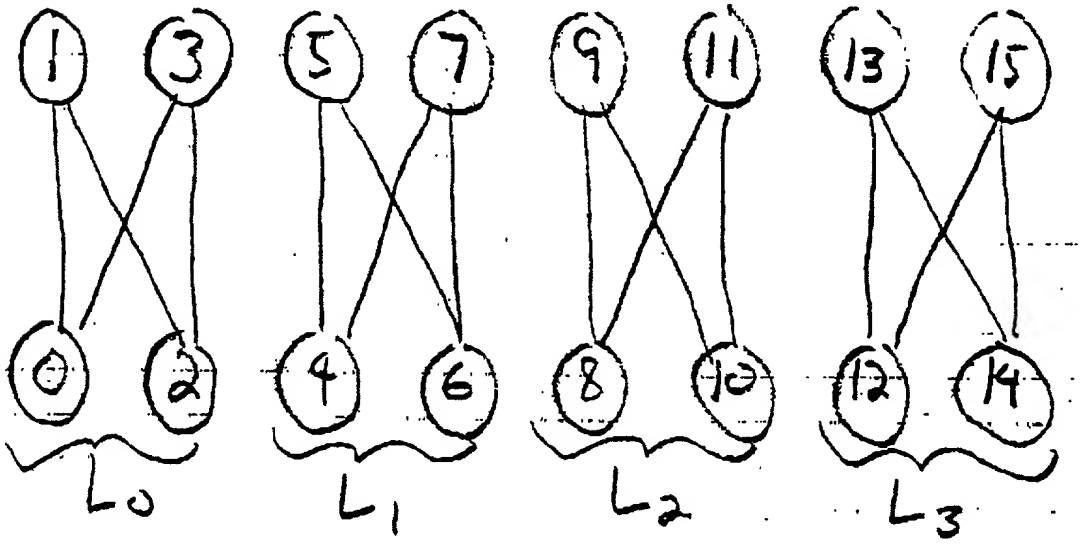


Figure 1a



Cube ring links

Figure 1b

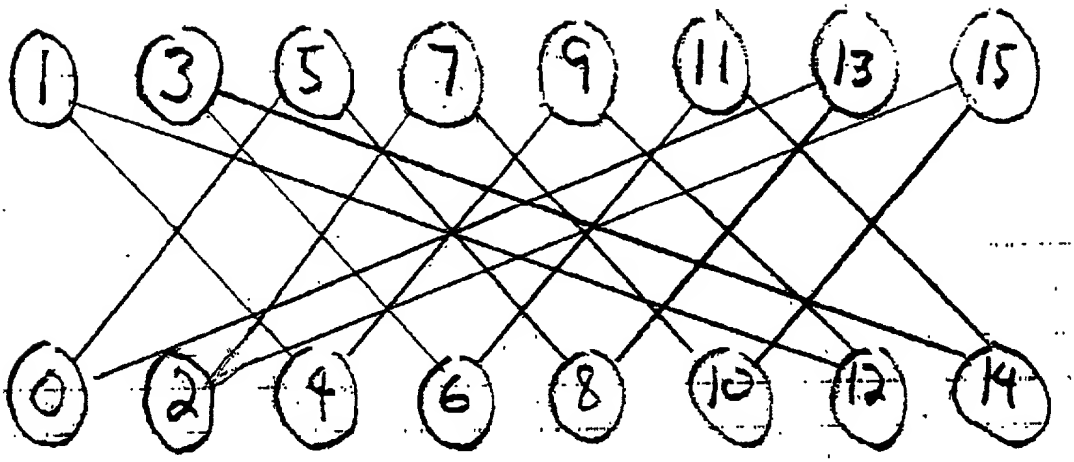
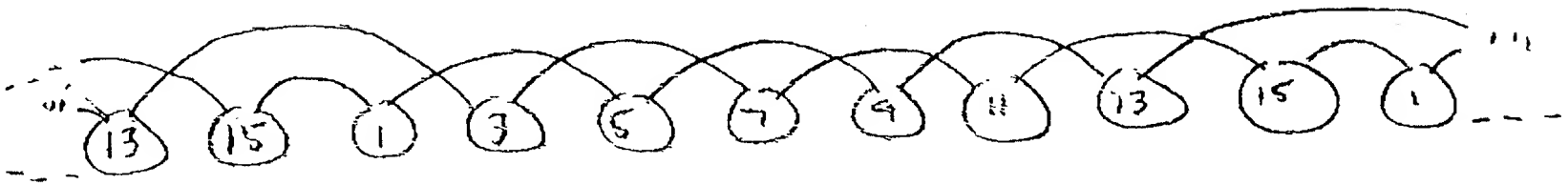


Figure 1C Parallel spanning links



I-ring

O-ring

Figure 1(d)

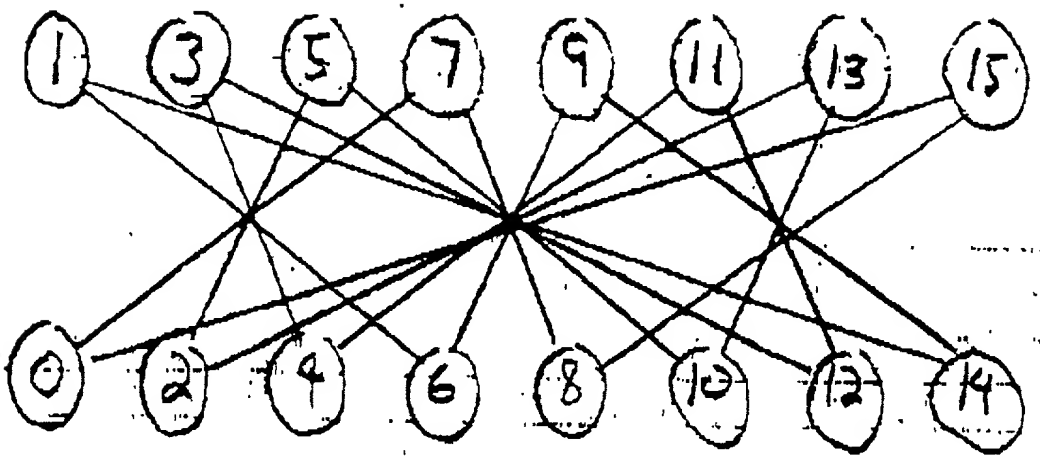


Figure 2 Twisted spanning links

Same core ring links as Figure 1

Same I-ring and O-ring links as Figure 1

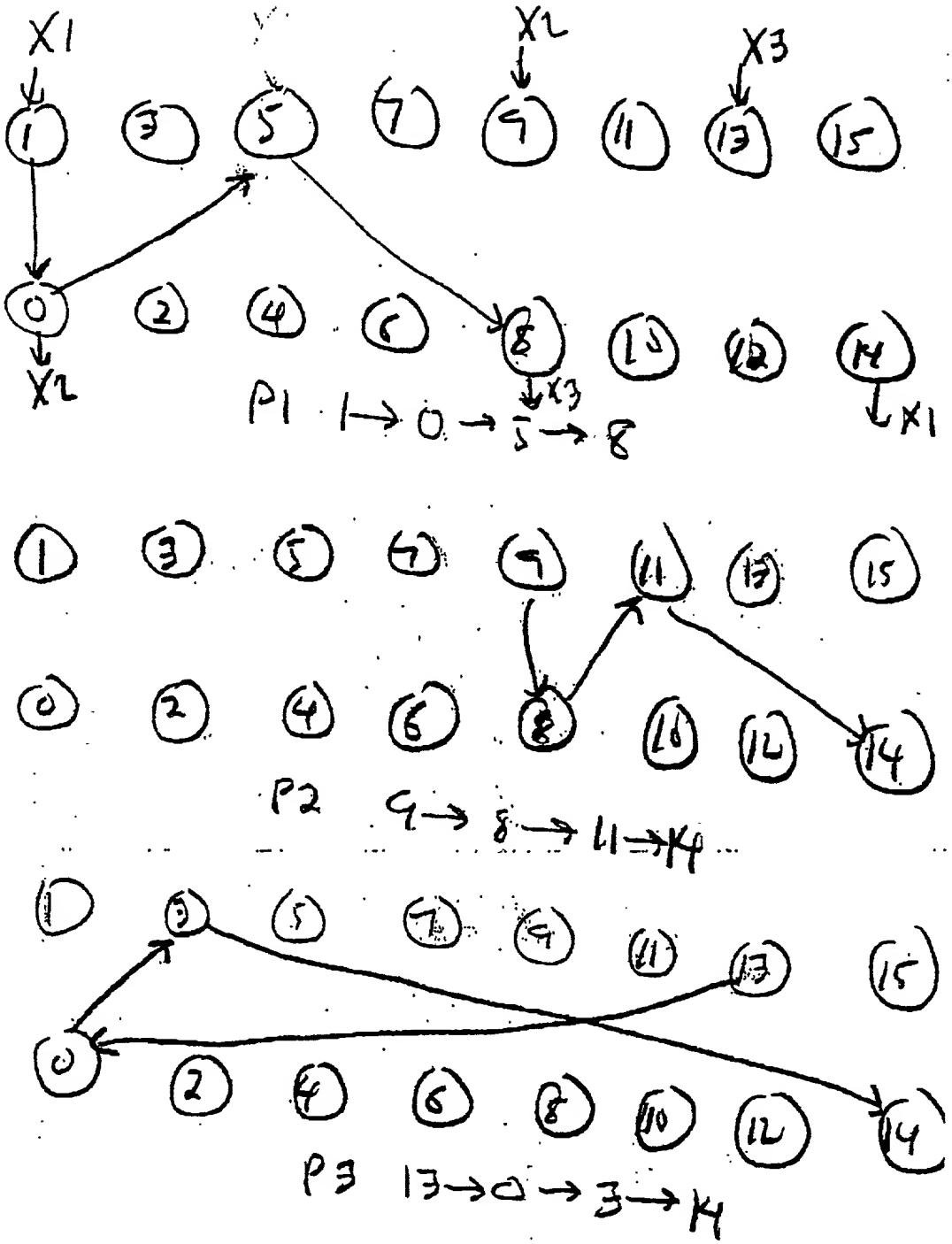


FIGURE 3

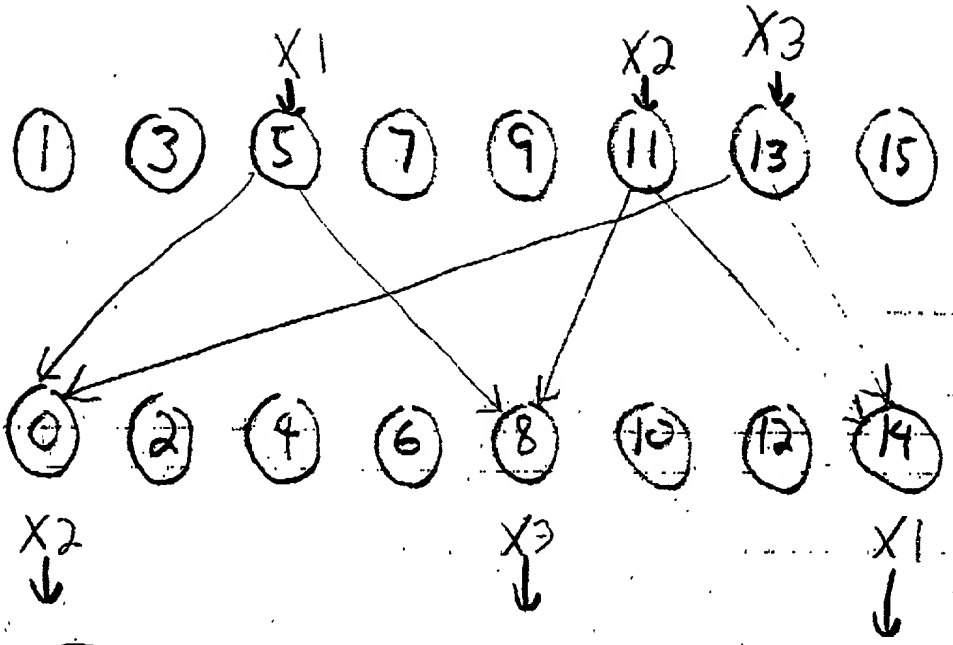


Figure 4 (b)

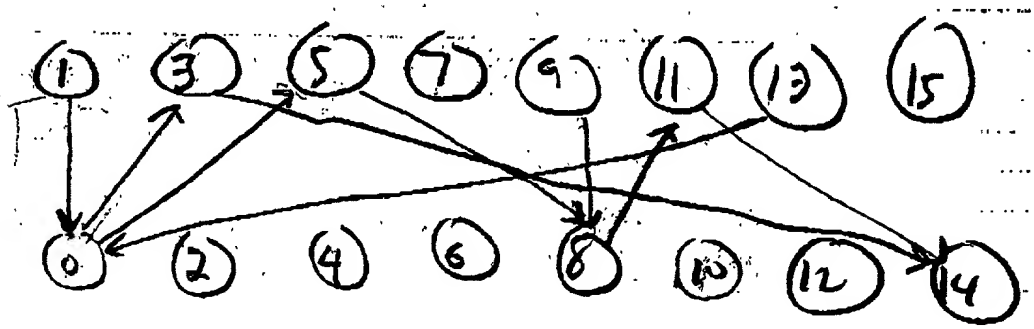
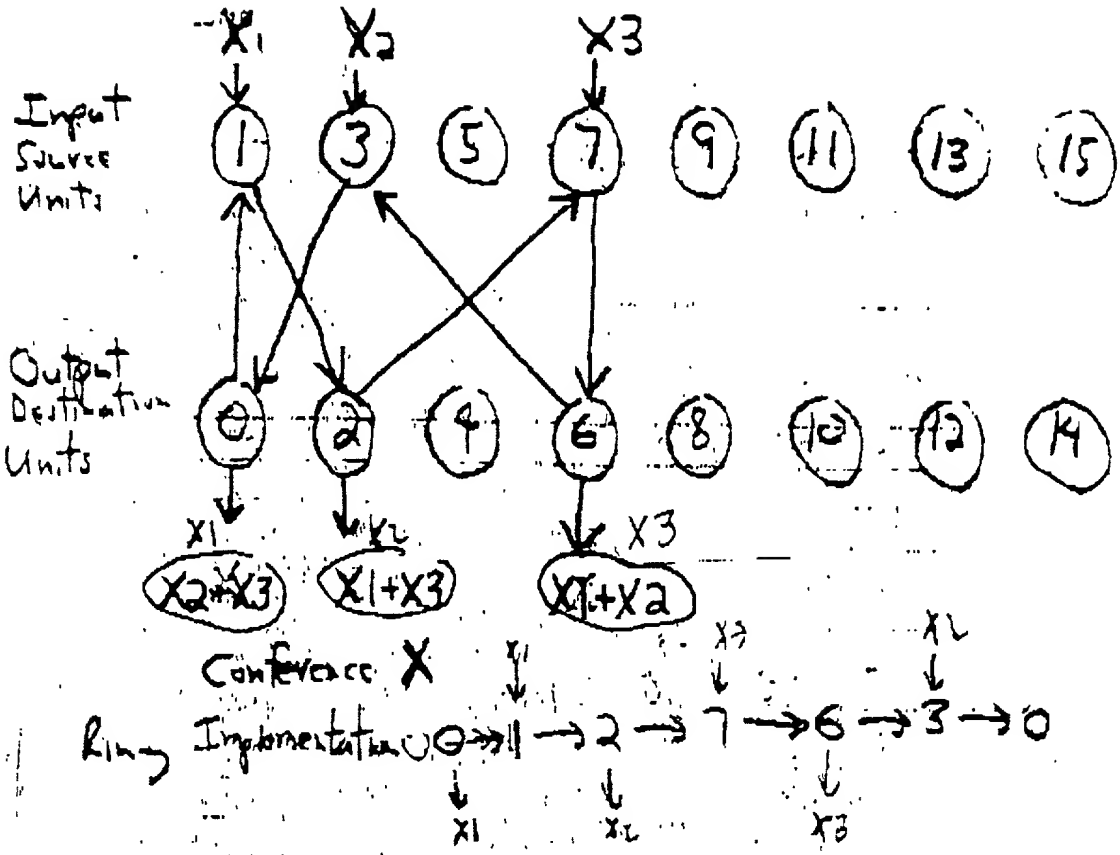
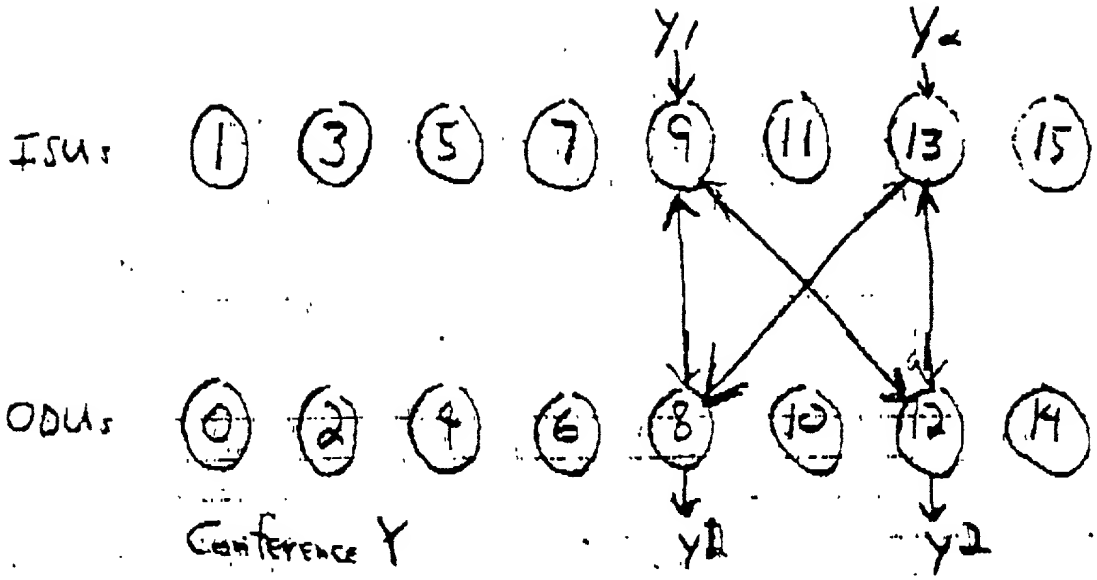


Figure 4(a)



3 party

Figure 5 (a)



Ring Implementation $8 \rightarrow 9 \rightarrow 12 \rightarrow 13 \rightarrow 8$

Figure 5 (1) 2 parts

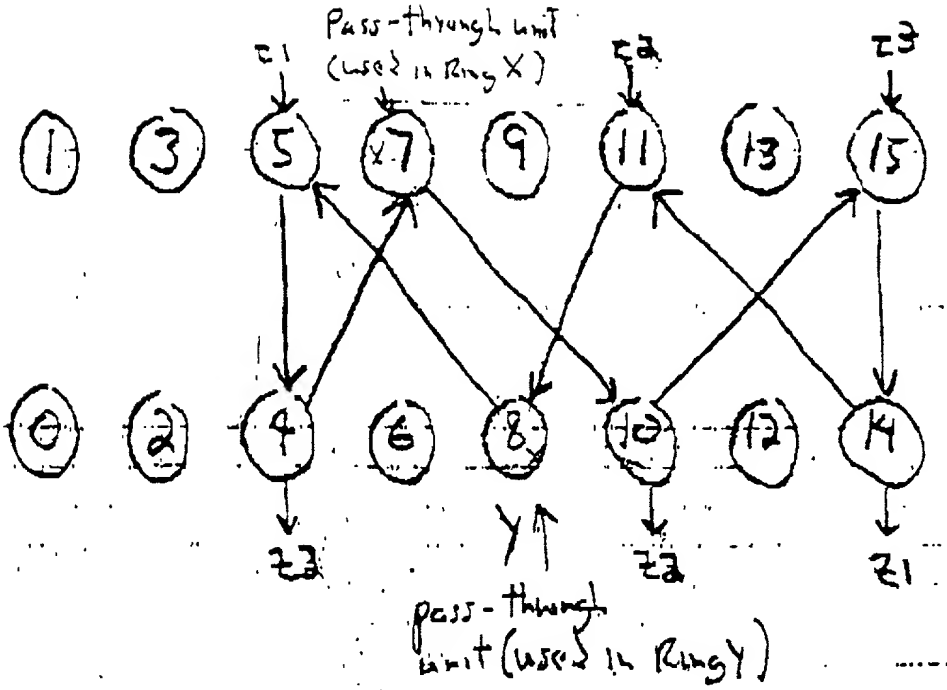
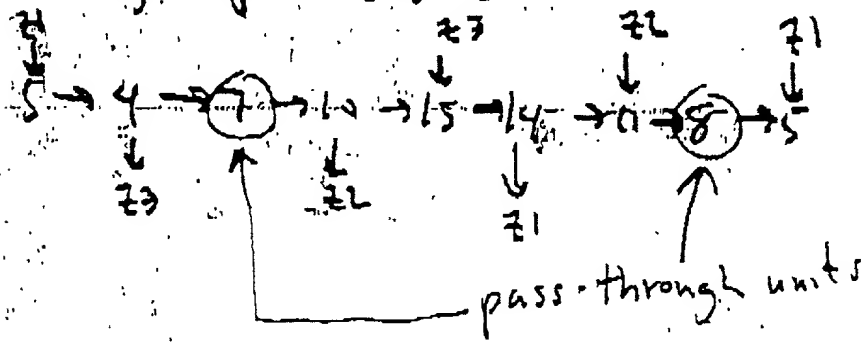
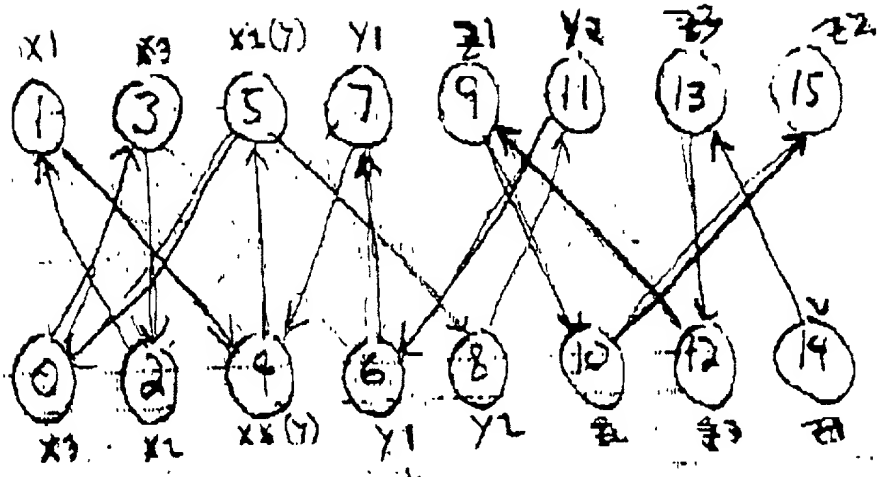


Figure 5 (c)
Conference Z
Ring Implementation





Ring X: 1 → 4 → 5 → 0 → 3 → 2 → 1

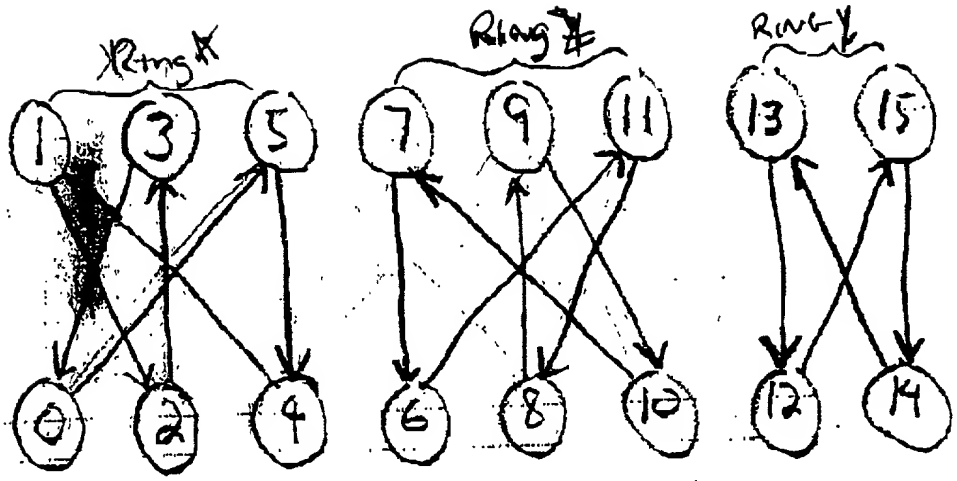
Ring Y: 7 → 4 → 5 → 8 → 11 → 6 → 7

Ring Z: 9 → 10 → 15 → 14 → 13 → 12 → 9

link 5 → 4 is a pass-through-unit for conf Y

nodes 5 & 4 are pass-through nodes for conf Y

Figure 6



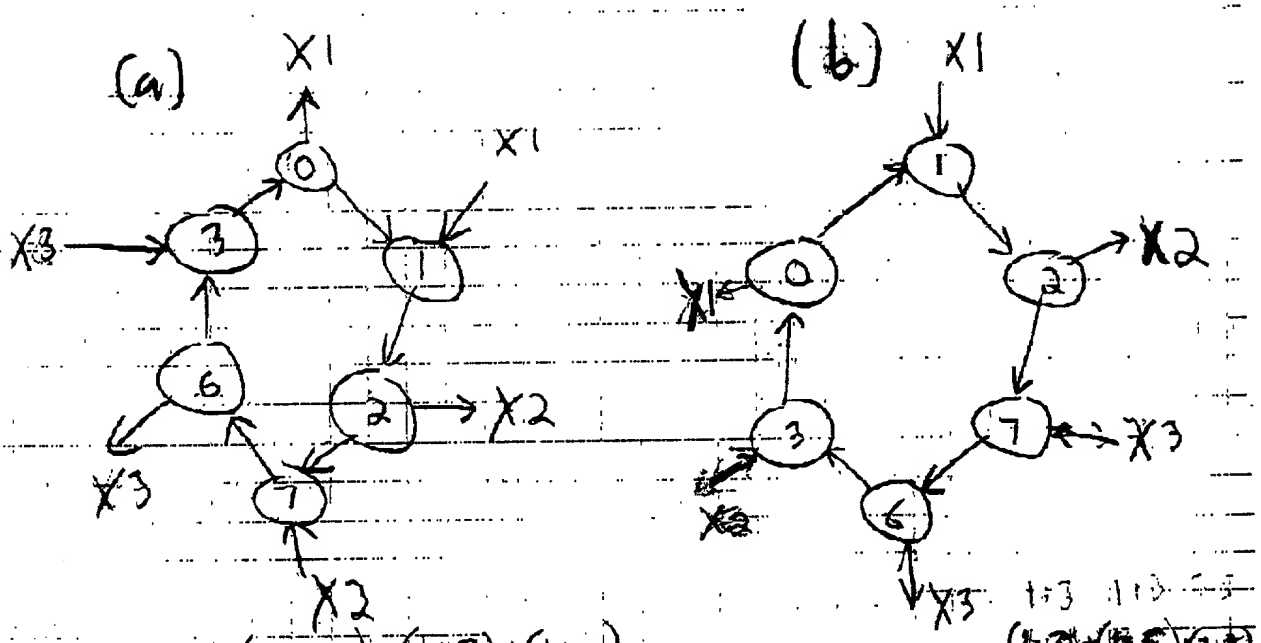
(3, 3, 2) ~~conf~~ Disjoint Implementation

X: $1 \to 2 \to 3 \to 0 \to 5 \to 4 \to 1$

Z: $11 \to 8 \to 9 \to 10 \to 7 \to 6 \to 11$

Y: $13 \to 12 \to 15 \to 14 \to 13$

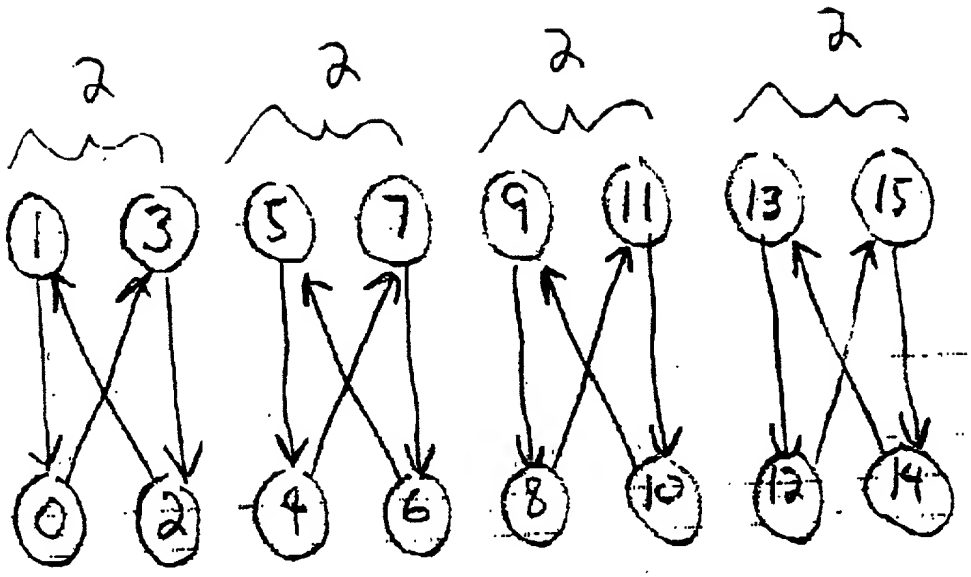
Figure 7



$$ALKD = \frac{(1+3)+(1+3)+(1+3)}{6} = 2$$

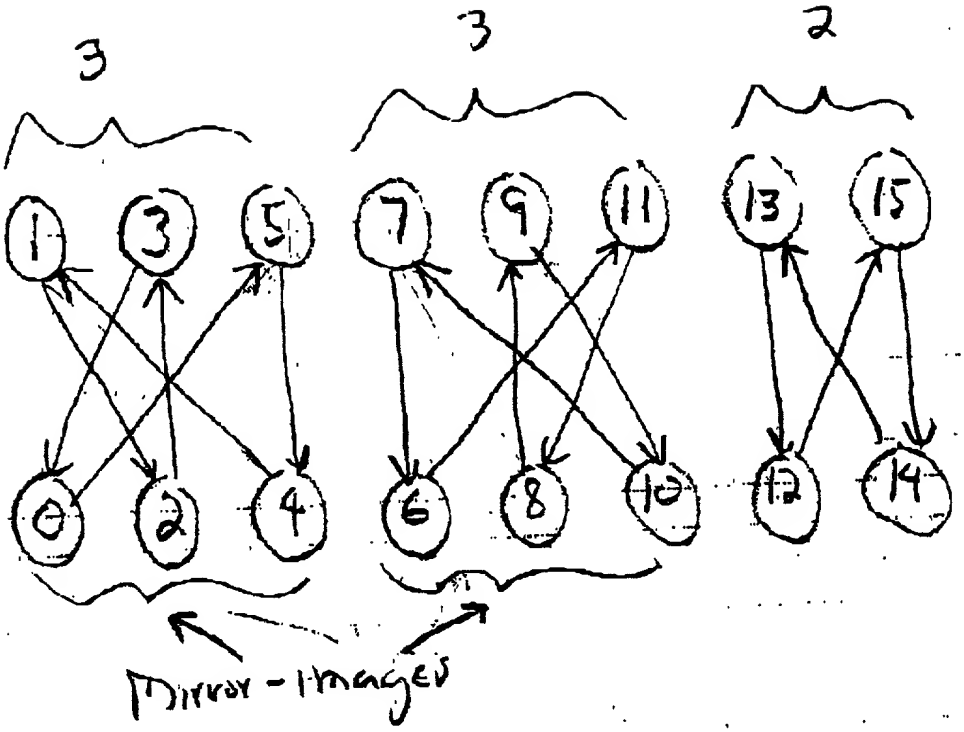
$$ALKD = \frac{(1+3)+(1+5)+(3+5)}{6} = \frac{18}{6} = 3$$

Figure 8



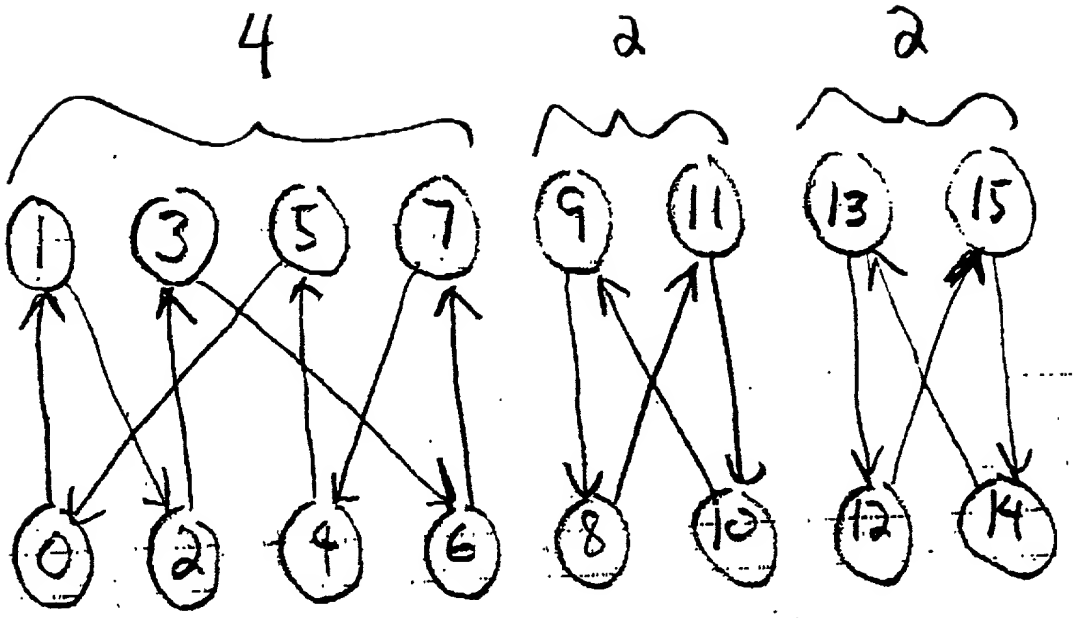
$(2,2,2,2)$-disjoint

Fig 9.(a)



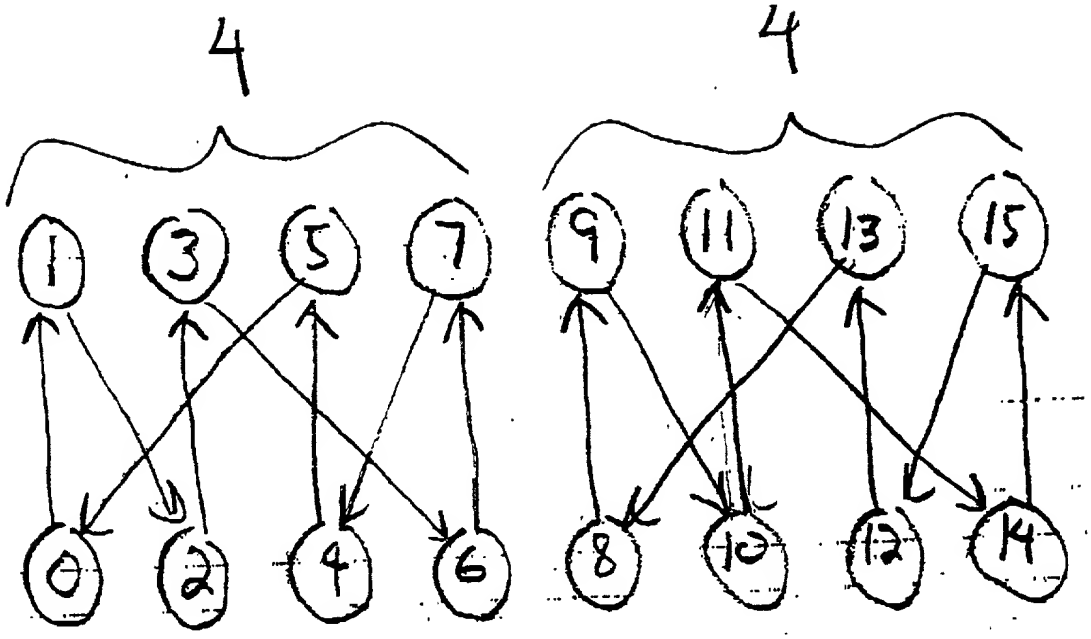
(3, 3, 2) - disjoint

Figure 9(1)



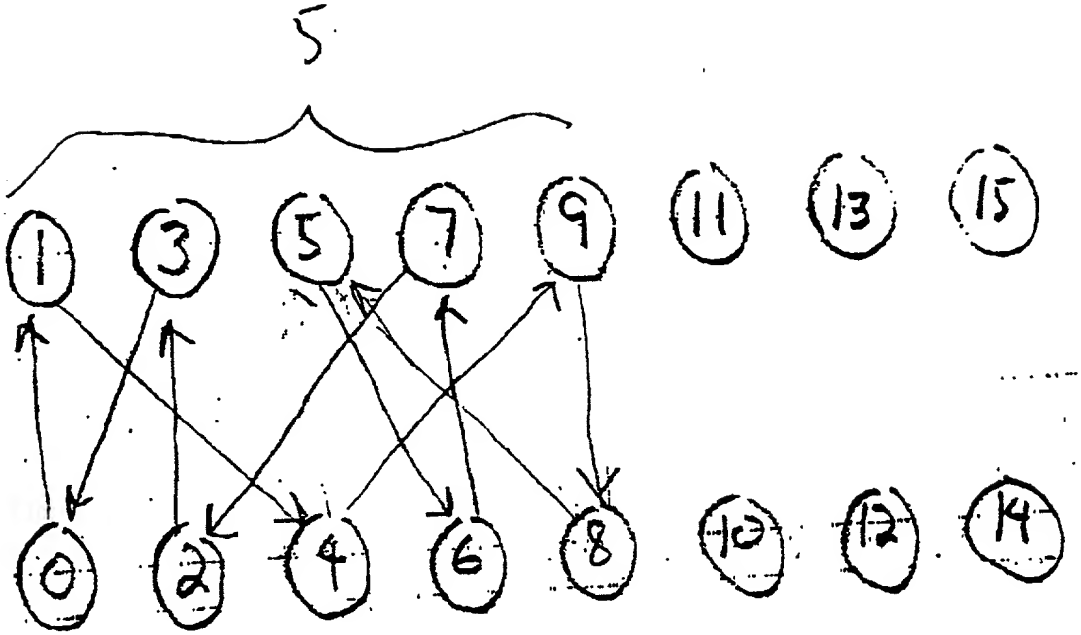
(4, 2, 2) - disjoint

Figure 9(c)



(4,4)-disjoint

Fig. 9(b)



alternative for the 10-node ring for the 5-party conference implementation in Fig. 9(e) for the (5,3)-Rijmen implementation example

Fig. 9(e)

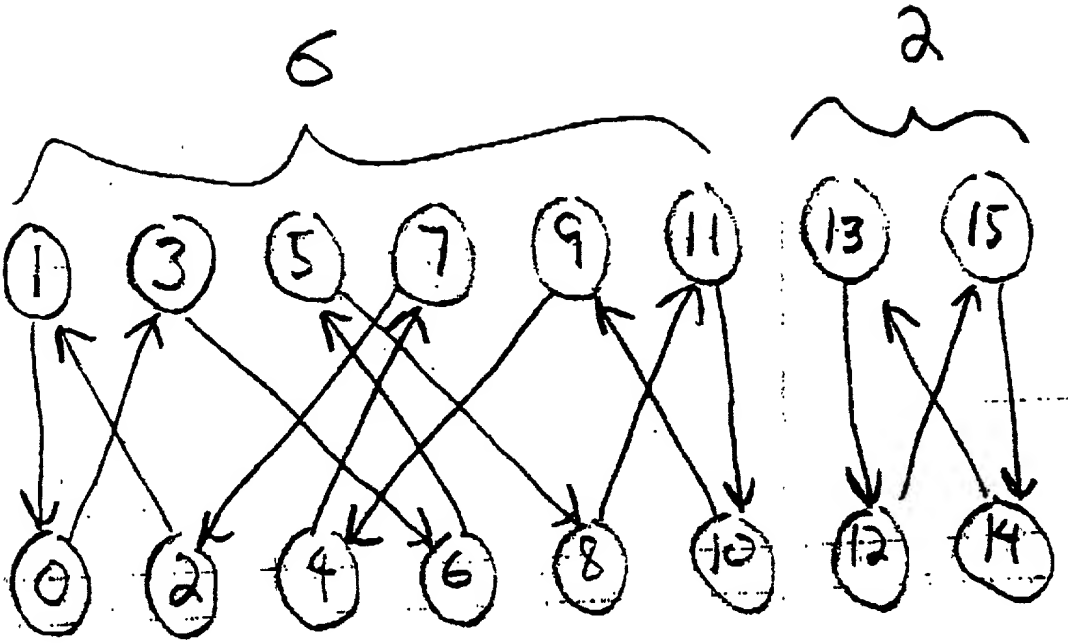
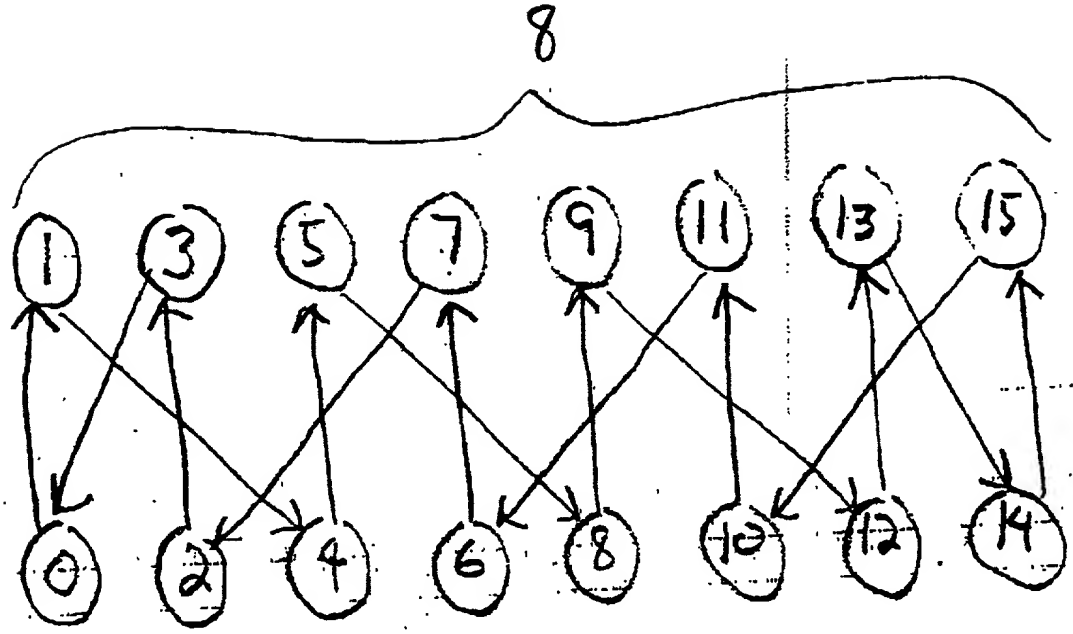
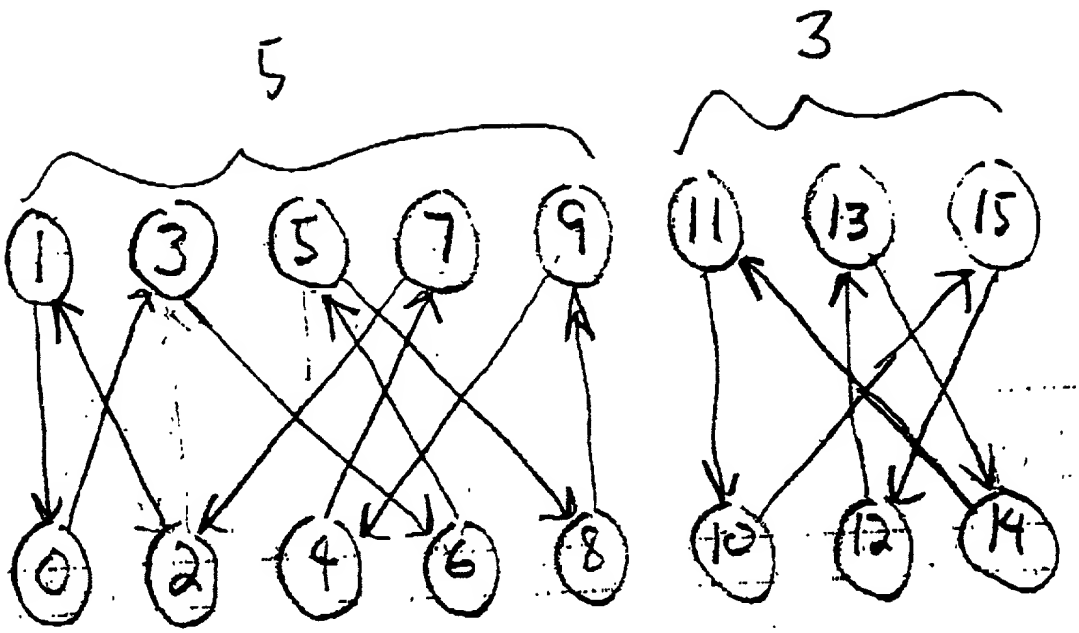


Fig. 9(f) (6,2) - disjoint



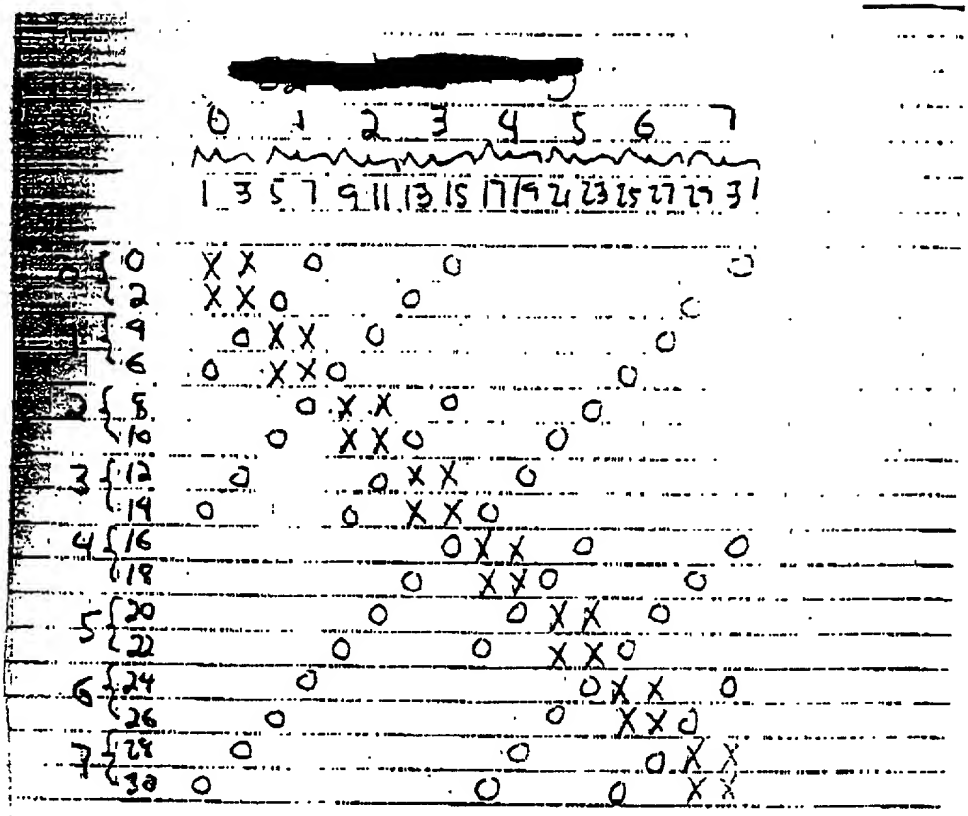
(8) - disjoint

Fig. 9(g)



(5, 3)-bijoint

Fig. 9(H)



The "X" indicates core ring links

The "O" indicates spanning ring links

~~32 node CX ring with only~~
twisted spanning links

Note that O-ring (even node - $\frac{1}{2}$ even node) links are not shown

Note that I-ring (odd node = $\frac{1}{2}$ odd node) links are not shown

Figure 10

	1	3	5	7	9	11	13	15
0		1, 3, (X, ϕ)	-1, 3, (X, ϕ)					
2	1, 3, (X, ϕ)	-1, 3, (X, ϕ)						
4	-1, 3, (X, ϕ)		(1, 5, (X, Y)	-1, 2, (Y, ϕ)				
6				1, 2, (Y, ϕ)		-1, 2, (Y, ϕ)		
8			1, 2 (Y, ϕ)			1, 2, (Y, ϕ)		
10					-1, 3, (Z, ϕ)			(-1, 3, (Z, ϕ)
12					(1, 3, (Z, ϕ)		-1, 3, (Z, ϕ)	
14							1, 3, (Z, ϕ)	-1, 3, (Z, ϕ)

$e(i,j) = (D_{i,j}, load_{i,j}, conf\text{-}assign(i,j) = (primary(i,j), pass\text{-}thru(i,j))$

Figure 11

	1	3	5	7	9	11	13	15
0		1, X	1, X					
2	-1, X	1, X						
4	1, X		-1, X					
6				-1, Y		1, Y		
8					1, Y	-1, Y		
10				1, Y	-1, Y			
12							-1, Z	1, Z
14							1, Z	-1, Z

Figure 12

0	2	4	6	8	10	12	14
ϕ, x_3, ϕ	ϕ, x_2, ϕ	ϕ, x_1, y	ϕ, y_1, ϕ	ϕ, y_2, ϕ	ϕ, z_2, ϕ	ϕ, z_3, ϕ	ϕ, z_1, ϕ

1	3	5	7	9	11	13	15
ϕ, x_1, ϕ	ϕ, x_3, ϕ	ϕ, x_2, y	ϕ, y_1, ϕ	ϕ, z_1, ϕ	ϕ, y_2, ϕ	ϕ, z_2, ϕ	ϕ, z_3, ϕ

Node-assignment(i) = (in(i), out(i), pass-thru(i))

Figure 13

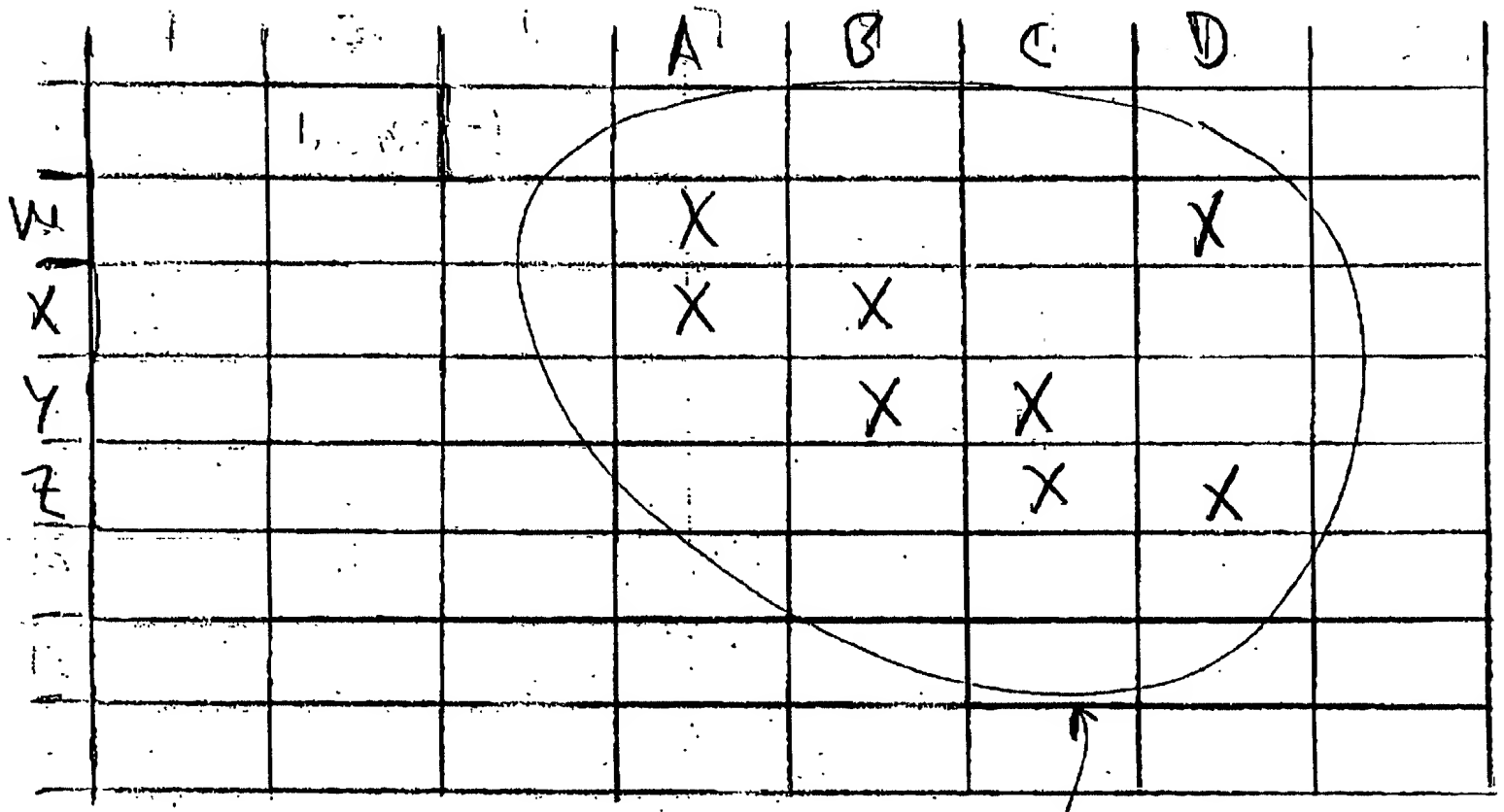


Figure 14(a)

Generic 8 node ring structure in a link indicator matrix

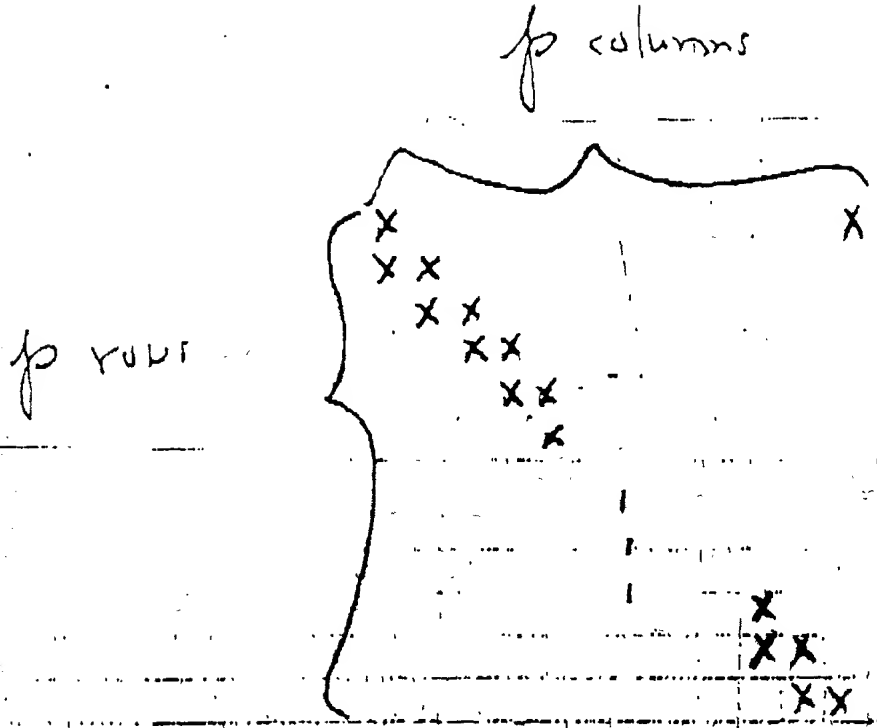


Figure 14(b)
Generic 2p node ring structure
in a link indicator matrix

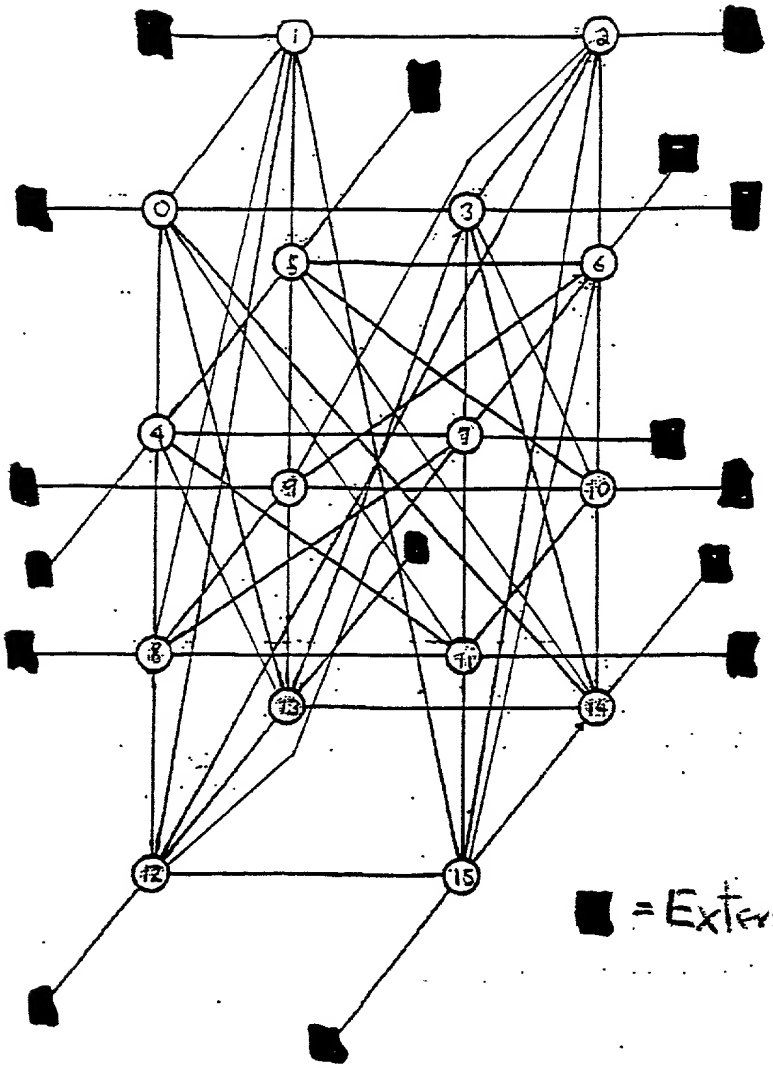


FIG
15

FIG 16a

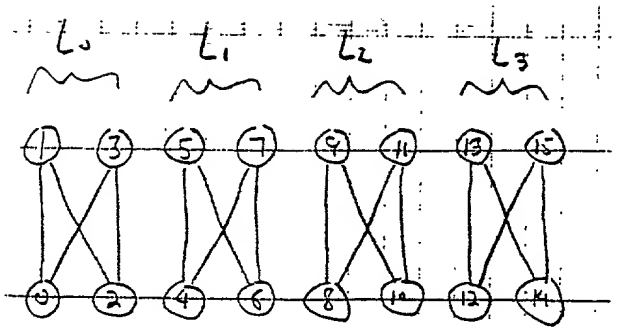


FIG 16b

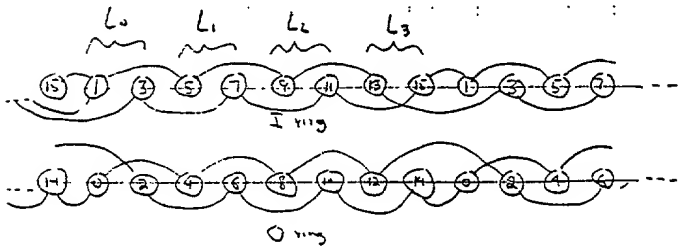
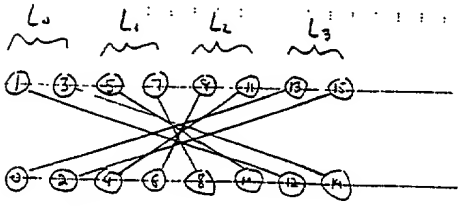
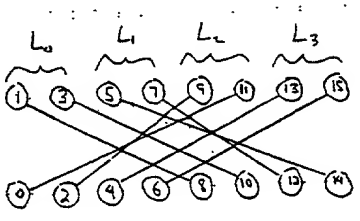


FIG 16 C



Type k=1 spanning links
Span breadth = $2^{k-1} = 1$
Twisted spanning pattern = {(5,10),(7,8),(9,6),(11,4)}
Parallel spanning pattern = {(1,12),(3,14),(13,0),(15,2)}



Type k=2 spanning links
Span breadth = $2^{k-1} = 2$
Twisted spanning pattern = {(15,14),(7,12),(9,2),(11,0)}
Parallel spanning pattern = {(1,8),(3,10),(13,4),(15,6)}

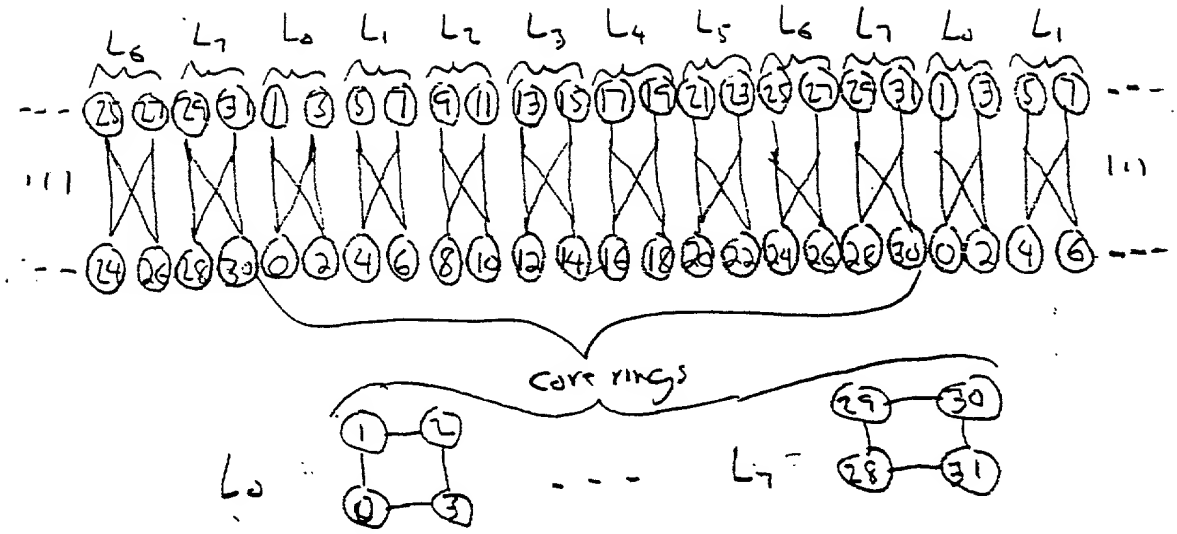


FIG 17

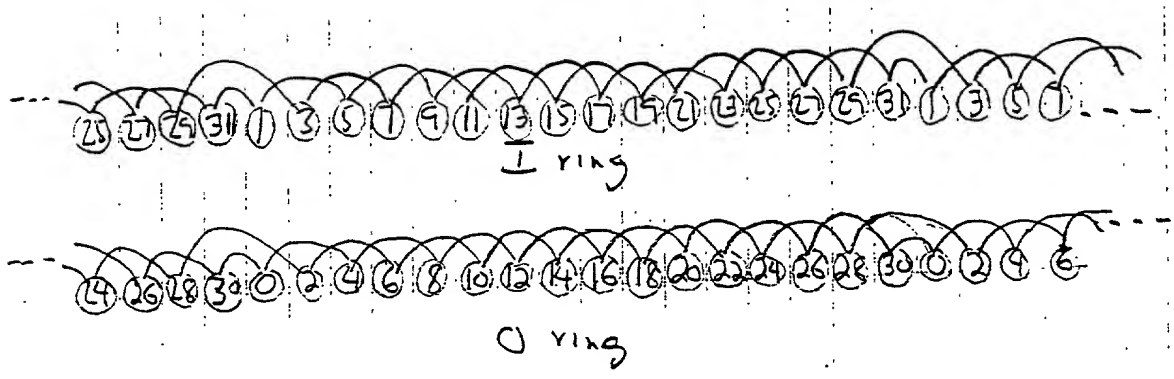


FIG 18

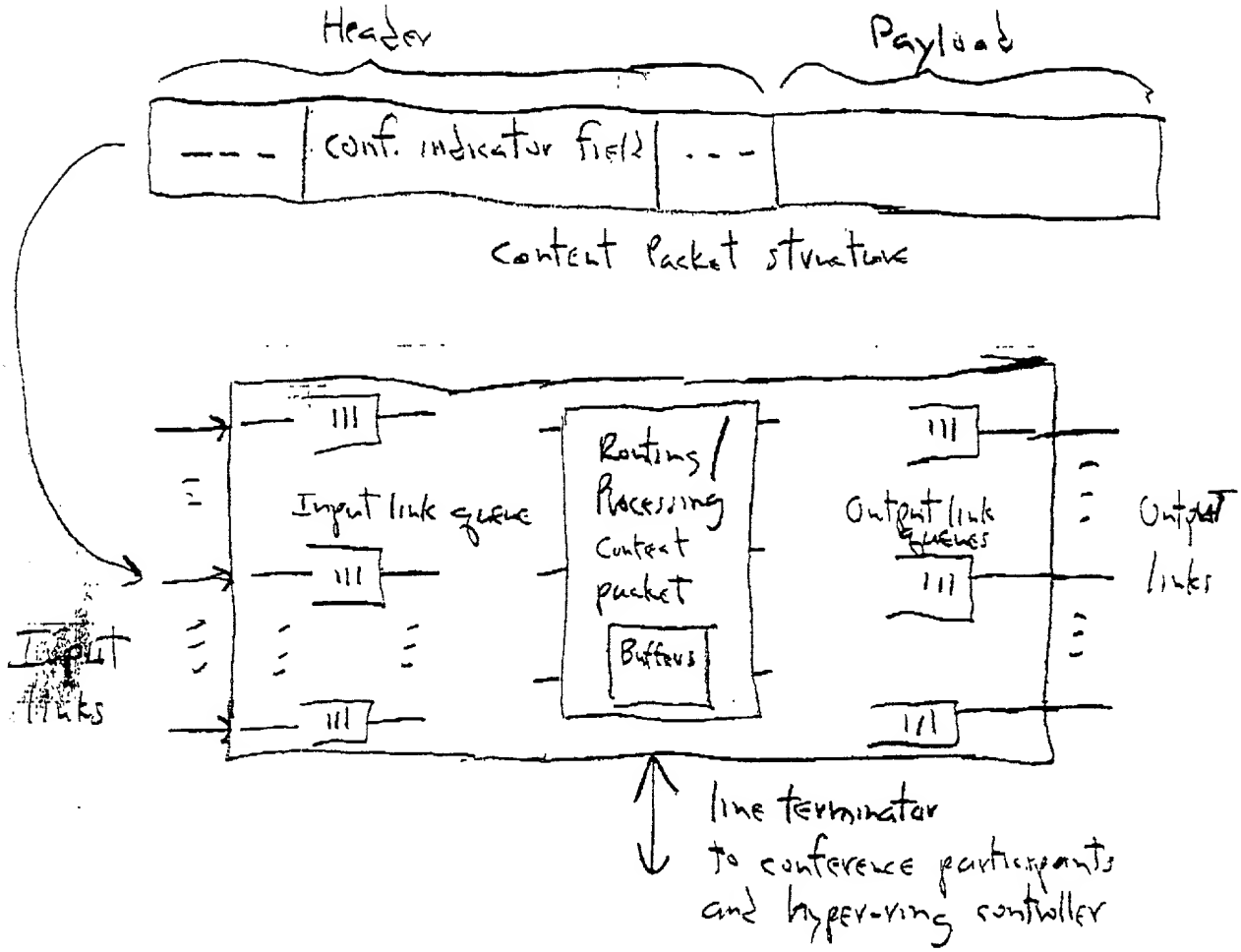

Header
Payload
conf. indicator field
Content Packet structure
Input link queue
Routing / Processing Content packet
Buffers
Output link queues
Output links
Input links
line terminator
to conference participants and hyperring controller

Figure 19

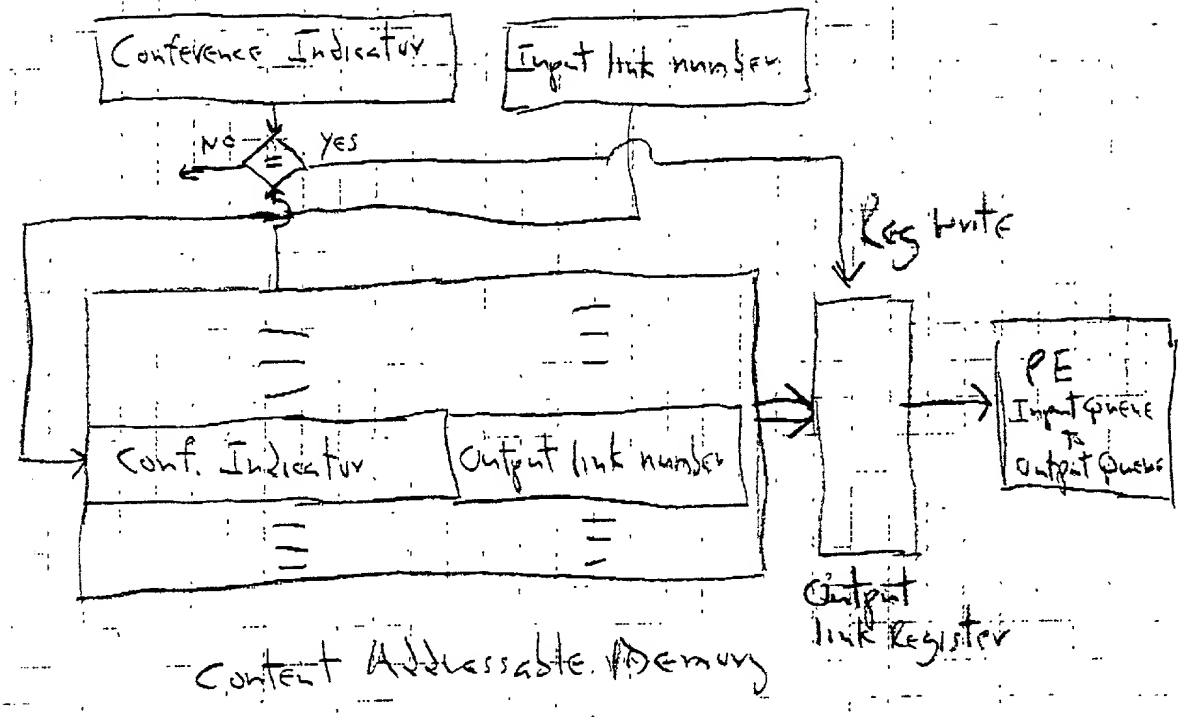

Conference Indicator
Input link number
NO
YES
Register
Conf. Indicator
Output link number
PE
Input Queue
To
Output Queue
Output
link Register
Content Addressable Memory

Figure 20

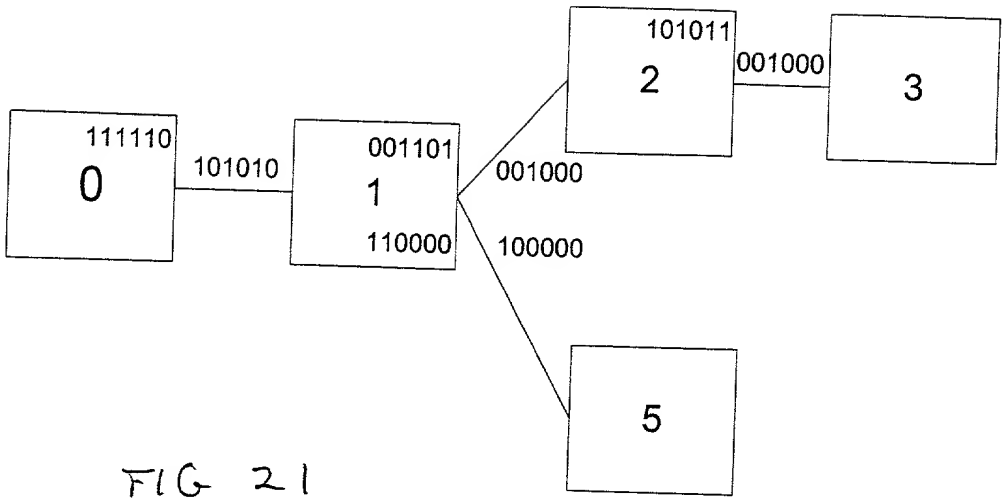

111110
0
101010
001101
1
110000
001000
100000
101011
2
001000
3
5

FIG 21

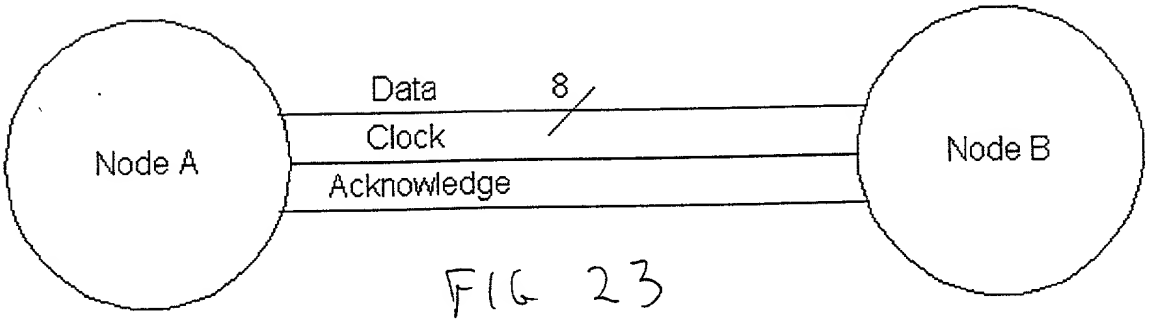

Node A
Data
8
Clock
Acknowledge
Node B

FIG 23

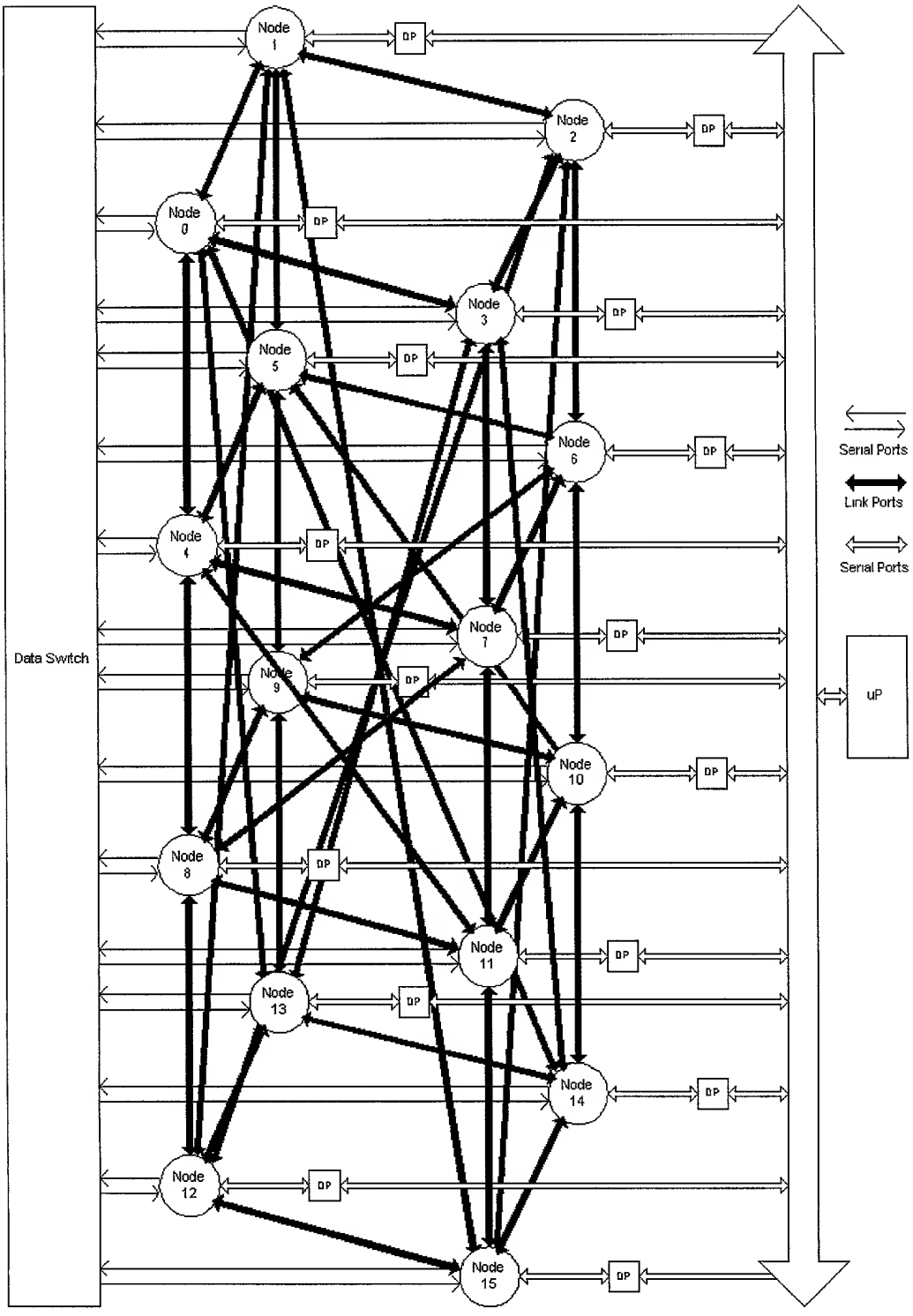

Node 1
Node 2
Node 0
Node 3
Node 5
Node 6
Node 4
Node 7
Node 9
Node 10
Node 8
Node 11
Node 13
Node 14
Node 12
Node 15
DP
Data Switch
Serial Ports
Link Ports
Serial Ports
uP

FIG 22

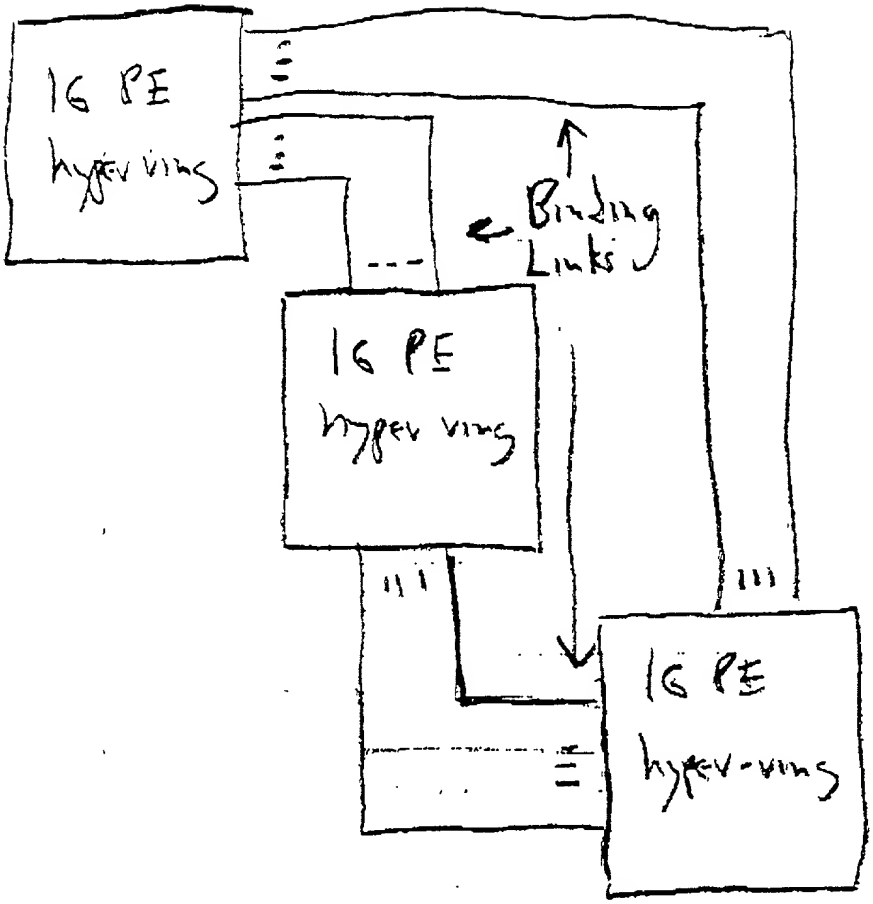

16 PE
hyper ving
Binding
Links
16 PE
hyper ving
16 PE
hyper-ving

Figure 24